Section 19 Electrical Characteristics

19.1 Absolute Maximum Ratings

Table 19-1 lists the absolute maximum ratings.

Table 19-1 Absolute Maximum Ratings

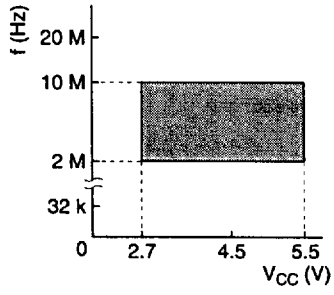
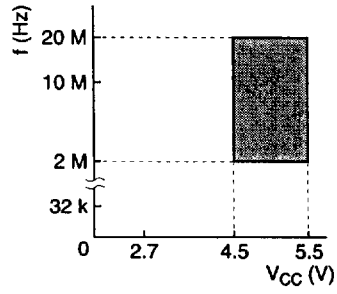
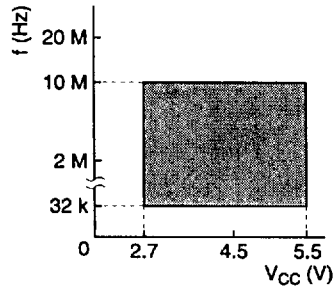
Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Programming voltage	V_{PP}	–0.3 to +13.5	V
Input voltage (except port 4)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (port 4)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

19.2 Power Supply Voltage and Operation Range

Table 19-2 shows the power supply voltage and operation range.

Table 19-2 Power Supply Voltage and Operation Range

Clock Supply	Module	Condition A	Condition B
Crystal resonator	All modules		
External clock input	DTC TPU SCI A/D converter		
	CPU Bus controller Interrupt controller I/O ports 8-bit timer WDT		

19.3 DC Characteristics

Table 19-3 lists the DC characteristics. Table 19-4 lists the permissible output currents.

Table 19-3 DC Characteristics: Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Port 2, $\overline{IRQ0}$ to $\overline{IRQ7}$	V_T^-	1.0	—	—	V	
		V_T^+	—	—	V_{CC} × 0.7	V	
		$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	V_{CC} – 0.7	—	V_{CC} +0.3	V	
	EXTAL		V_{CC} × 0.7	—	V_{CC} +0.3	V	
	Port 1, 3, 5, A to G		2.0	—	V_{CC} +0.3	V	
	Port 4		2.0	—	AV_{CC} +0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	0.5	V	
	NMI, EXTAL, Port 1, 3 to 5, A to G		–0.3	—	0.8	V	
Output high voltage	All output pins	V_{OH}	V_{CC} –0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Port 1, A to C		—	—	1.0	V	I_{OL} = 10 mA
Input leakage current	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	I_{in}	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} –0.5 V
	Port 4		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} –0.5 V

Note: 1. If the A/D converter is not used, do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{ref} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 19-3 DC Characteristics: Conditions:V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current (off state)	Port 1 to 3, 5, A to G	$\|I_{TSI}\|$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} –0.5 V
Input pull-up MOS current	Port A to E	$-I_P$	50	—	300	µA	V_{in} = 0 V
Input capacitance	$\overline{RES}$	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	NMI		—	—	50	pF	
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	
Current dissipation*[2]	Normal operation	I_{CC}*[4]	—	50 (5.0 V)	75 (5.5 V)	mA	f = 20 MHz
	Sleep mode		—	35 (5.0 V)	55 (5.5 V)	mA	f = 20 MHz
	All module stop mode		—	35 (5.0 V)	—	mA	Reference value f = 20 MHz
	Medium speed (φ/32) mode		—	25 (5.0 V)	—	mA	Reference value f = 20 MHz
	Sleep, all module stop and medium speed (φ/32) mode		—	5.0 (5.0 V)	10 (5.5 V)	mA	f = 20 MHz
	Standby mode*[3]		—	0.01	5.0	µA	$T_a \leq 50°C$
			—	—	20.0		50°C < T_a
Analog power supply current	During A/D conversion	AI_{CC}	—	1.2	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference current	During A/D conversion	AI_{CC}	—	0.5	0.8	mA	V_{ref} = 5.0 V
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D converter is not used, do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{ref} to V_{CC}, and connect AV_{SS} to V_{SS}.

2. Current dissipation values are for V_{IH} min = V_{CC} –0.5 V and V_{IL} max = 0.5V with all output pins unloaded and the on-chip pull-up transistors in the off state.

3. The values are for $V_{RAM} \leq V_{CC} < 4.5V$, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.

4. I_{CC} depends on V_{CC} and f as follows:

   I_{CC} max = 2.0 (mA) + 0.67 (mA/(MHz × V)) × V_{CC} × f [normal mode]

   I_{CC} max = 2.0 (mA) + 0.48 (mA/(MHz × V)) × V_{CC} × f [sleep mode]

   I_{CC} max = 2.0 (mA) + 0.07 (mA/(MHz × V)) × V_{CC} × f [sleep, all module stop and medium speed (ϕ/32) mode]

Table 19-3 DC Characteristics: Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Port 2, $\overline{IRQ0}$ to $\overline{IRQ7}$	V_T^-	$V_{CC} \times 0.2$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} +0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Port 1, 3, 5, A to G		$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Port4		$V_{CC} \times 0.7$	—	AV_{CC} +0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, Port 1, 3 to 5, A to G		–0.3	—	$V_{CC} \times 0.2$	V	V_{CC} < 4.0 V
					0.8		V_{CC} = 4.0 to 5.5 V
Output high voltage	All output pins	V_{OH}	V_{CC} –0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} –1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Port 1, A to C		—	—	1.0	V	$V_{CC} \leq 4$ V I_{OL} = 5 mA 4 V < $V_{CC} \leq 5$ V I_{OL} = 10 mA
Input leakage current	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} –0.5V
	Port 4		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} –0.5V

Note: 1. If the A/D converter is not used, do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{ref} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 19-3 DC Characteristics: Conditions:V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current (off state)	Port 1 to 3, 5, A to G	$\|I_{TSI}\|$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} –0.5 V
Input pull-up current	Port A to E	$-I_P$	10	—	300	µA	V_{CC} = 2.7 V to 5.5 V, V_{in} = 0 V
Input capacitance	$\overline{RES}$	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, Ta = 25°C
	NMI		—	—	50	pF	
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	
Current dissipation*[2]	Normal operation	I_{CC}*[4]	—	13 (3.0 V)	40 (5.5 V)	mA	f = 10 MHz
			—	60	120	µA	f = 32 kHz, V_{CC} = 3.0 V
	Sleep mode		—	9 (3.0 V)	28 (5.5 V)	mA	f = 10 MHz
	All module stop mode		—	9 (3.0 V)	—	mA	Reference value f = 10 MHz
	Medium speed (φ/32) mode		—	6 (3.0 V)	—	mA	Reference value f = 10 MHz
	Sleep, all module stop and medium speed (φ/32) mode		—	1.5 (3.0 V)	6.0 (5.5 V)	mA	f = 10 MHz
			—	30	60	µA	f = 32 kHz, V_{CC} = 3.0 V
	Standby mode*[3]		—	0.01	5.0	µA	$T_a \leq 50°C$
			—	—	20.0		50°C < T_a
Analog power supply current	During A/D conversion	AI_{CC}	—	0.4	1.0	mA	AV_{CC} = 3.0 V
			—	1.2	—	mA	AV_{CC} = 5.0 V
	Idle		—	0.01	5.0	µA	

Table 19-3 DC Characteristics: Conditions:V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Reference power supply current	During A/D conversion	AI_{CC}	—	0.3	0.6	mA	V_{ref} = 3.0 V
			—	0.5	—	mA	V_{ref} = 5.0 V
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D converter is not used, do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{ref} to V_{CC}, and connect AV_{SS} to V_{SS}.

2. Current dissipation values are for V_{IH} min = V_{CC} –0.5 V and V_{IL} max = 0.5V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3V.
4. I_{CC} depends on V_{CC} and f as follows:
   I_{CC} max = 2.0 (mA) + 0.67 (mA/(MHz× V)) × V_{CC} × f [normal mode]
   I_{CC} max = 2.0 (mA) + 0.48 (mA/(MHz× V)) × V_{CC} × f [sleep mode]
   I_{CC} max = 2.0 (mA) + 0.07 (mA/(MHz× V)) × V_{CC} × f [sleep, all module stop and medium speed (ϕ/32) mode]

Table 19-4 Permissible Output Currents: Conditions:V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to +75°C (regular specifications), Ta = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Port1, A to C	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 28 pins including port 1 and A to C	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 19-4.

2. When driving a darlington pair or LED, always insert a current-limiting resister in the output line, as show in figures 19-1 and 19-2.

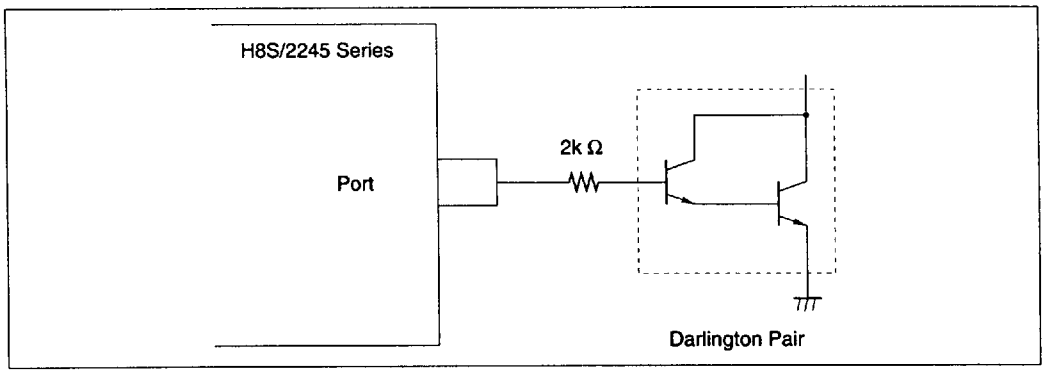


Figure 19-1 Darlington Pair Drive Circuit (Example)

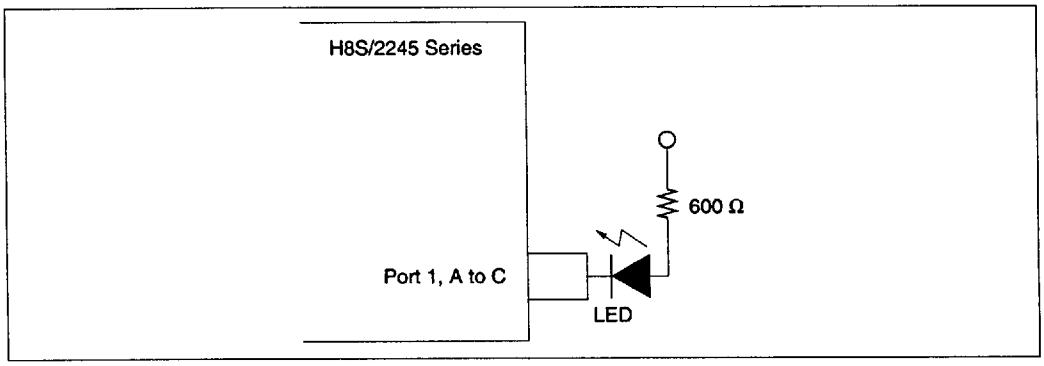


Figure 19-2 LED Drive Circuit (Example)

19.4 AC Characteristics

Figure 19-3 show, the test conditions for the AC characteristics.

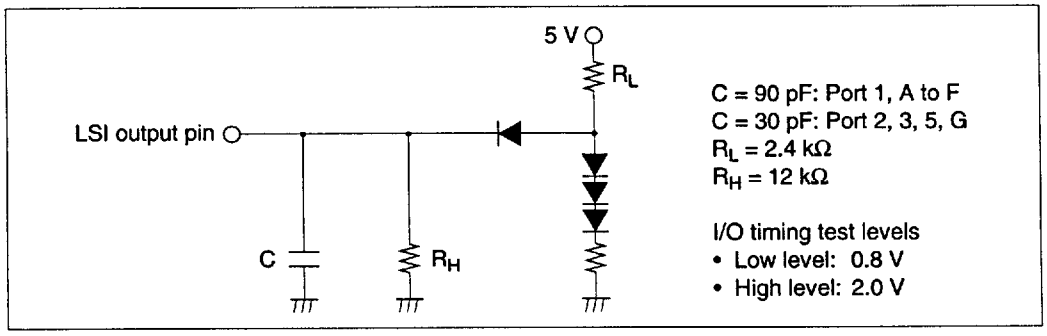


Figure 19-3 Output Load Circuit

19.4.1 Clock Timing

Table 19-5 lists the clock timing

Table 19-5 Clock Timing

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ϕ = 32 kHz to 10 MHz, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)
Condition B: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ϕ = 2 to 20 MHz, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
Clock cycle time	t_{cyc}	100	31250	50	500	ns	Figure 19-4
Clock high pulse width	t_{CH}	35	—	20	—	ns	Figure 19-4
Clock low pulse width	t_{CL}	35	—	20	—	ns	
Clock rise time	t_{Cr}	—	15	—	5	ns	
Clock fall time	t_{Cf}	—	15	—	5	ns	
Clock oscillator setting time at reset (crystal)	t_{OSC1}	20	—	10	—	ms	Figure 19-5
Clock oscillator setting time in software standby (crystal)	t_{OSC2}	20	—	10	—	ms	
External clock output stabilization delay time	t_{DEXT}	500	—	500	—	µs	

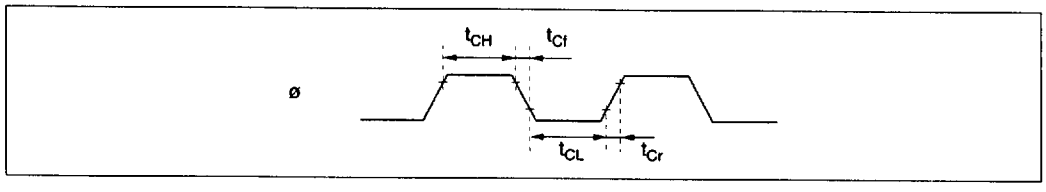


Figure 19-4 System Clock Timing

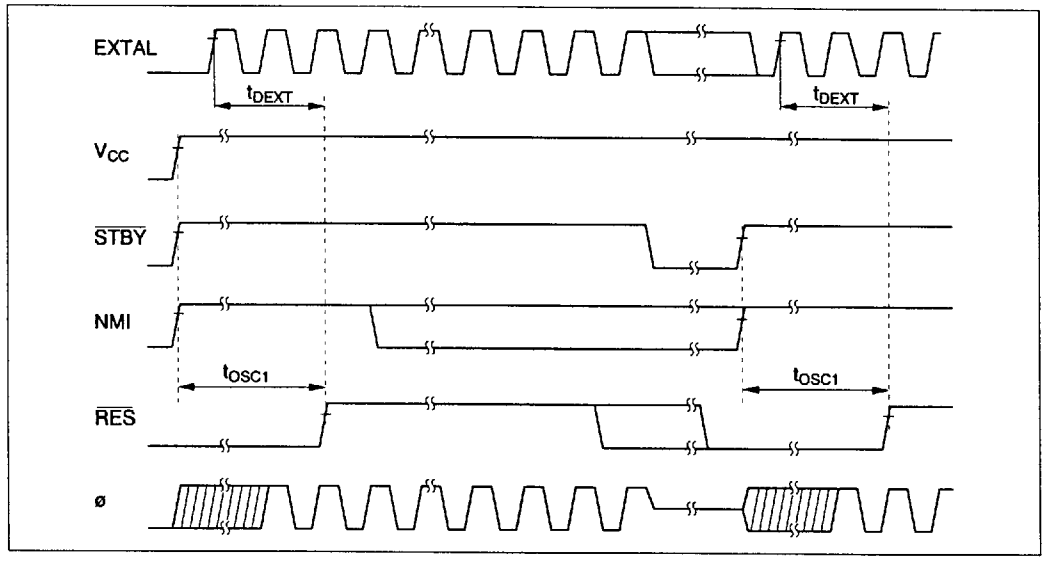


Figure 19-5 Oscillator Settling Timing

19.4.2 Control Signal Timing

Table 19-6 lists the control signal timing.

Table 19-6 Control Signal Timing

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ϕ = 32 kHz to 10 MHz, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)
Condition B: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ϕ = 2 to 20 MHz, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 19-6
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI reset setup time	t_{NMIRS}	200	—	200	—	ns	
NMI reset hold time	t_{NMIRH}	200	—	200	—		
NMI setup time	t_{NMIS}	200	—	150	—	ns	Figure 19-7
NMI hold time	t_{NMIH}	10	—	10	—		
NMI pulse width (exiting software standby mode)	t_{NMIW}	200	—	200	—	ns	
$\overline{IRQ}$ setup time	t_{IRQS}	200	—	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—	10	—	ns	
$\overline{IRQ}$ pulse width (exiting software standby mode)	t_{IRQW}	200	—	200	—	ns	

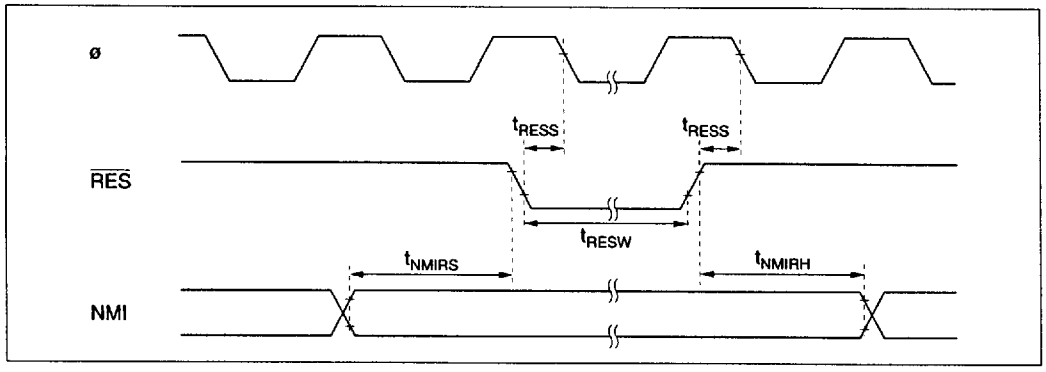


Figure 19-6 Reset Input Timing

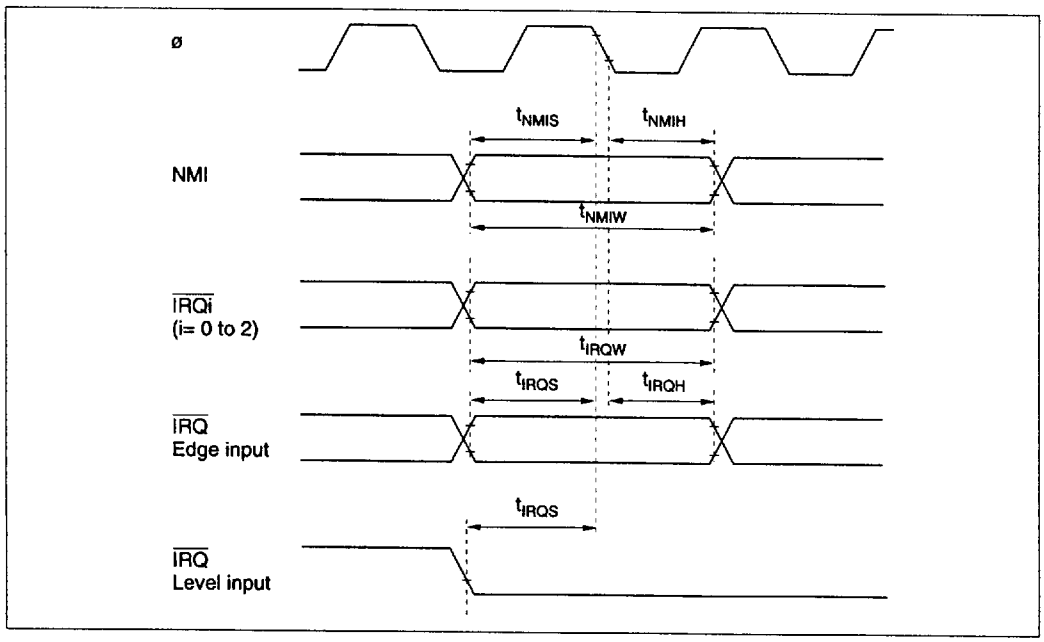


Figure 19-7 Interrupt Input Timing

19.4.3 Bus Timing

Table 19-7 lists the bus timing.

Table 19-7 Bus Timing

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ϕ = 32 kHz to 10 MHz, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)
Condition B: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ϕ = 2 to 20 MHz, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
Address delay time	t_{AD}	—	40	—	20	ns	Figure 19-8 to Figure 19-12
Address setup time	t_{AS}	0.5 × t_{cyc} – 30	—	0.5 × t_{cyc} – 15	—	ns	
Address hold time	t_{AH}	0.5 × t_{cyc} – 20	—	0.5 × t_{cyc} – 10	—	ns	
$\overline{CS}$ delay time	t_{CSD}	—	40	—	20	ns	
$\overline{AS}$ delay time	t_{ASD}	—	60	—	30	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	60	—	30	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	60	—	30	ns	
Read data setup time	t_{RDS}	30	—	15	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	1.0 × t_{cyc} – 50	—	1.0 × t_{cyc} – 25	ns	
Read data access time 2	t_{ACC2}	—	1.5 × t_{cyc} – 50	—	1.5 × t_{cyc} – 25	ns	
Read data access time 3	t_{ACC3}	—	2.0 × t_{cyc} – 50	—	2.0 × t_{cyc} – 25	ns	
Read data access time 4	t_{ACC4}	—	2.5 × t_{cyc} – 50	—	2.5 × t_{cyc} – 25	ns	
Read data access time 5	t_{ACC5}	—	3.0 × t_{cyc} – 50	—	3.0 × t_{cyc} – 25	ns	

Table 19-7 Bus Timing (cont)

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32 kHz to 10 MHz, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)
Condition B: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 to 20 MHz, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
$\overline{WR}$ delay time 1	t_{WRD1}	—	60	—	30	ns	Figure 19-8 to Figure 19-12
$\overline{WR}$ delay time 2	t_{WRD2}	—	60	—	30	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	1.0 × t_{cyc} – 40	—	1.0 × t_{cyc} – 20	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	1.5 × t_{cyc} – 40	—	1.5 × t_{cyc} – 20	—	ns	
Write data delay time	t_{WDD}	—	60	—	30	ns	
Write data setup time	t_{WDS}	0	—	0	—	ns	
Write data hold time	t_{WDH}	20	—	10	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	60	—	30	—	ns	Figure 19-10
$\overline{WAIT}$ hold time	t_{WTH}	10	—	5	—	ns	
$\overline{BREQ}$ setup time	t_{BRQS}	60	—	30	—	ns	Figure 19-13
$\overline{BACK}$ delay time	t_{BACD}	—	60	—	30	ns	
Bus-floating time	t_{BZD}	—	100	—	50	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	60	—	30	ns	Figure 19-14

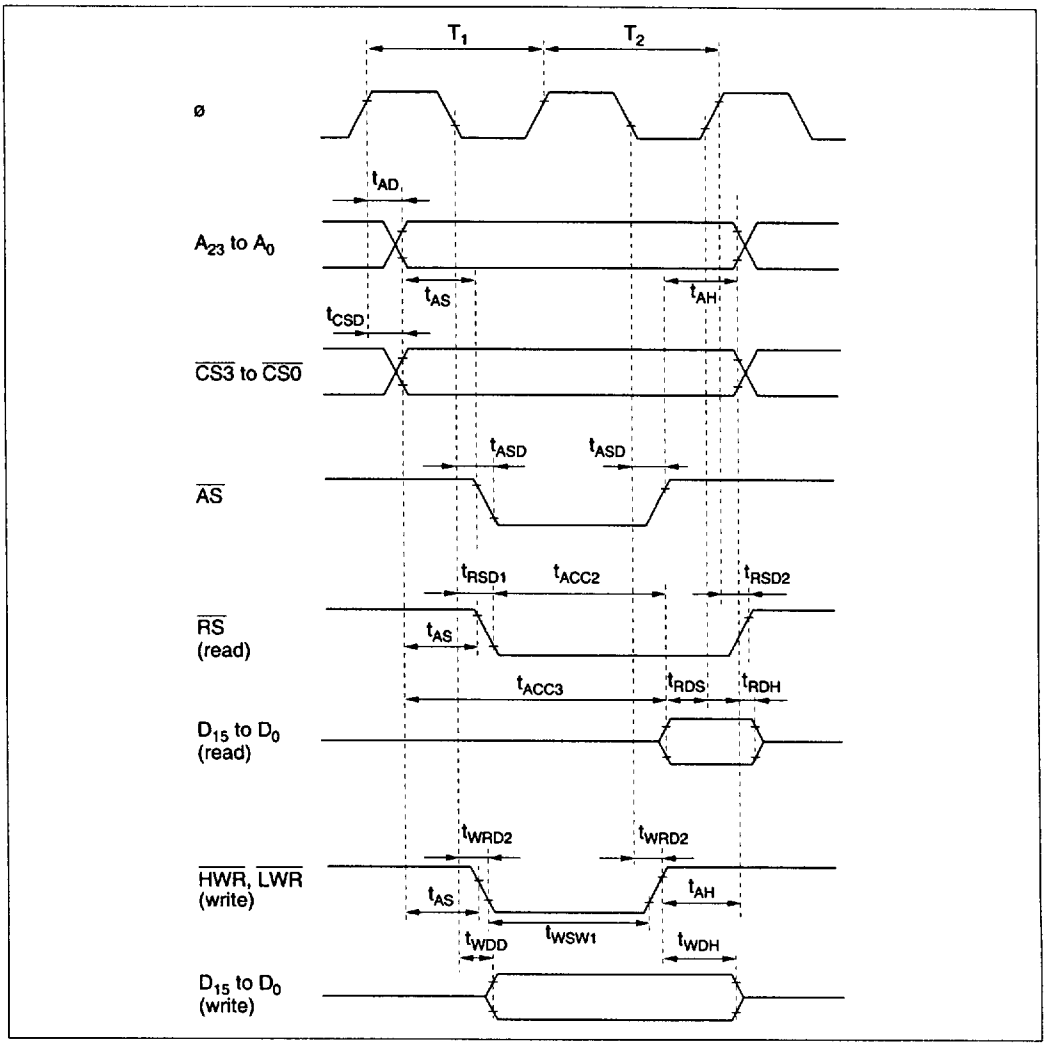


Figure 19-8 Basic Bus Timing (Two-State Access)

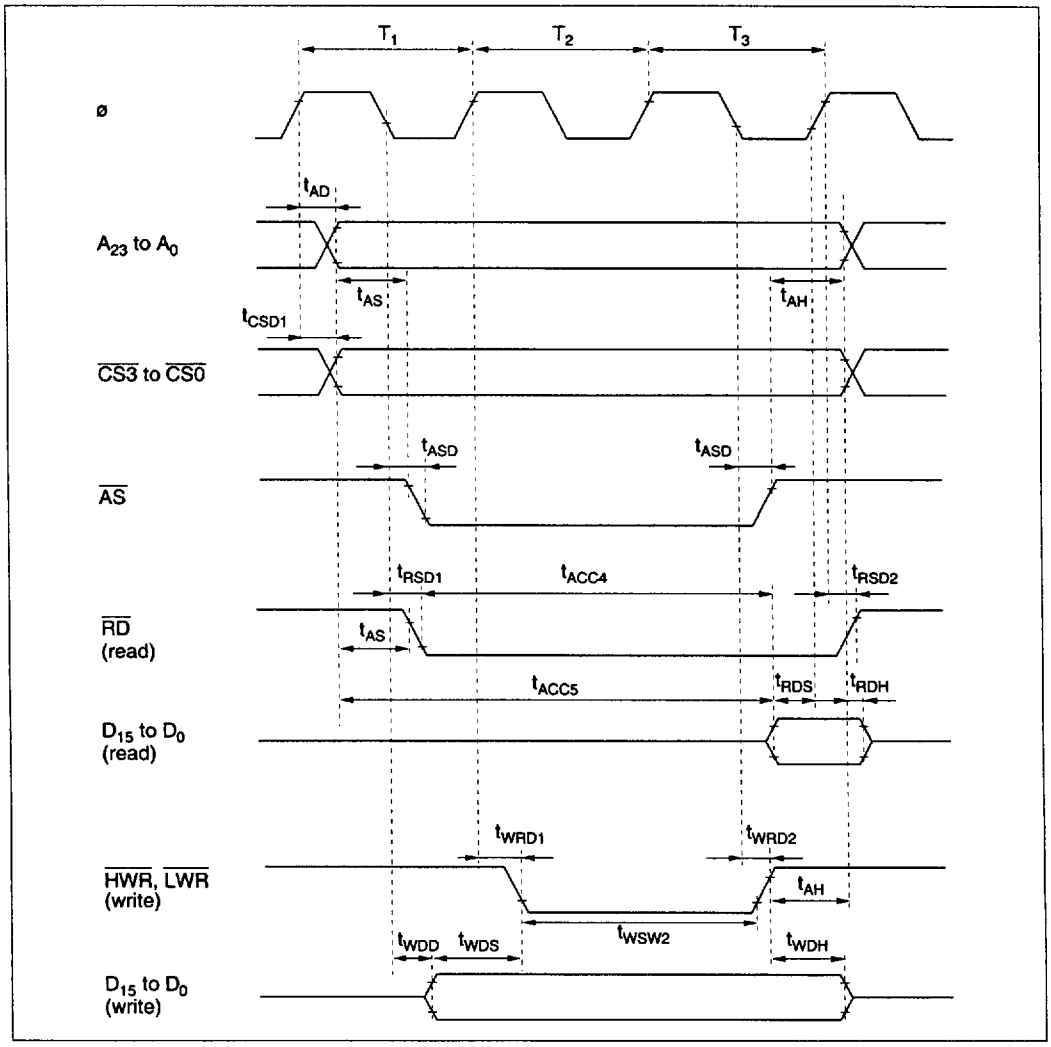


Figure 19-9 Basic Bus Timing (Three-State Access)

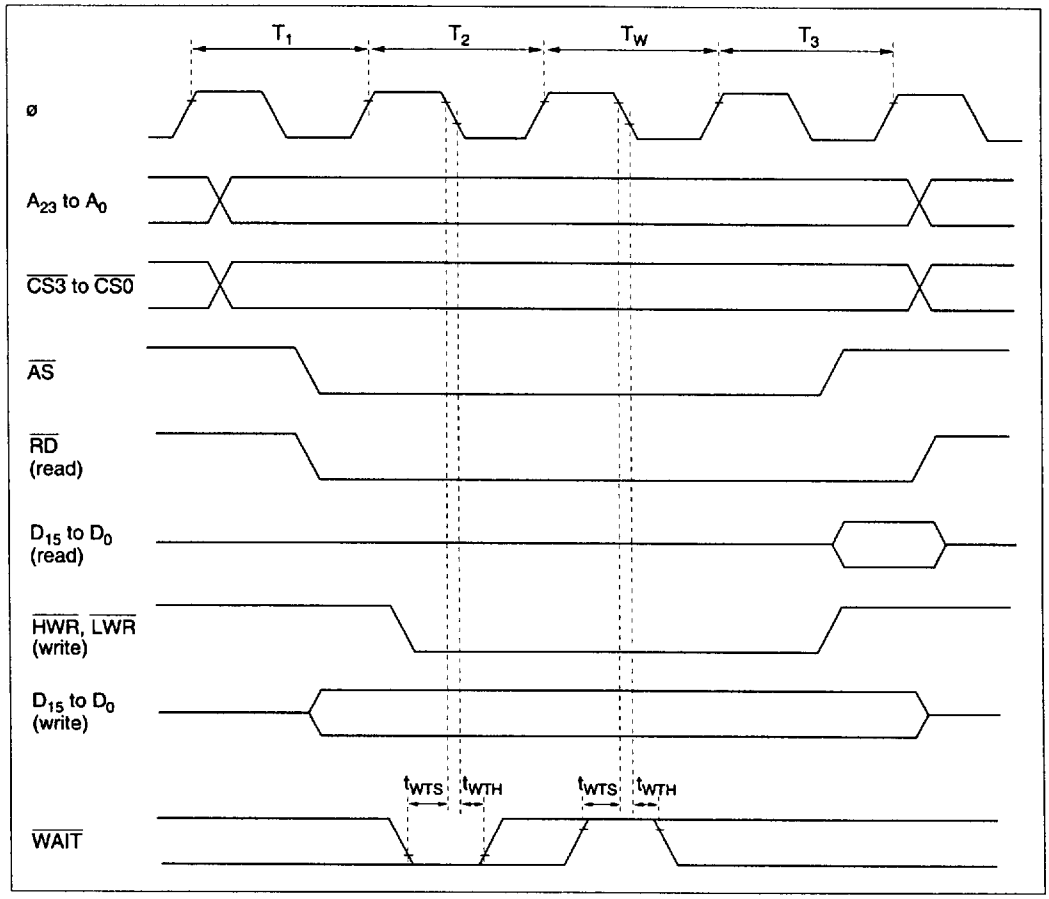


Figure 19-10 Basic Bus Timing (Three-State Access with One Wait State)

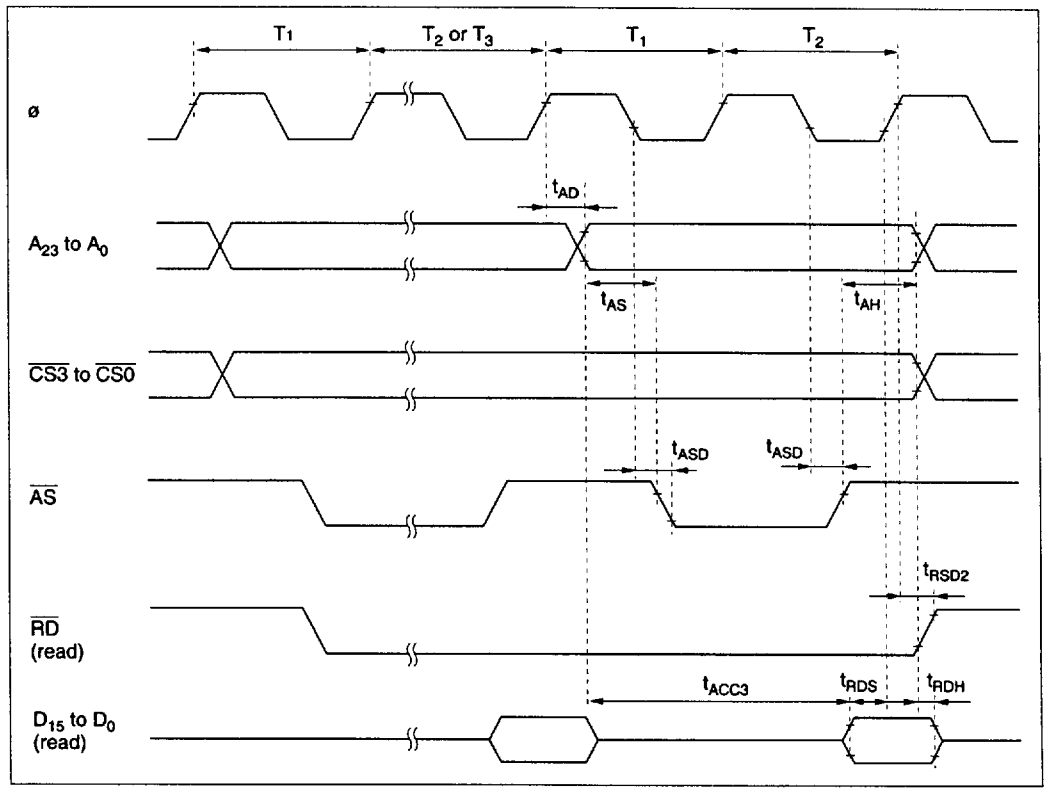


Figure 19-11 Burst ROM Access Timing (Two-State Access)

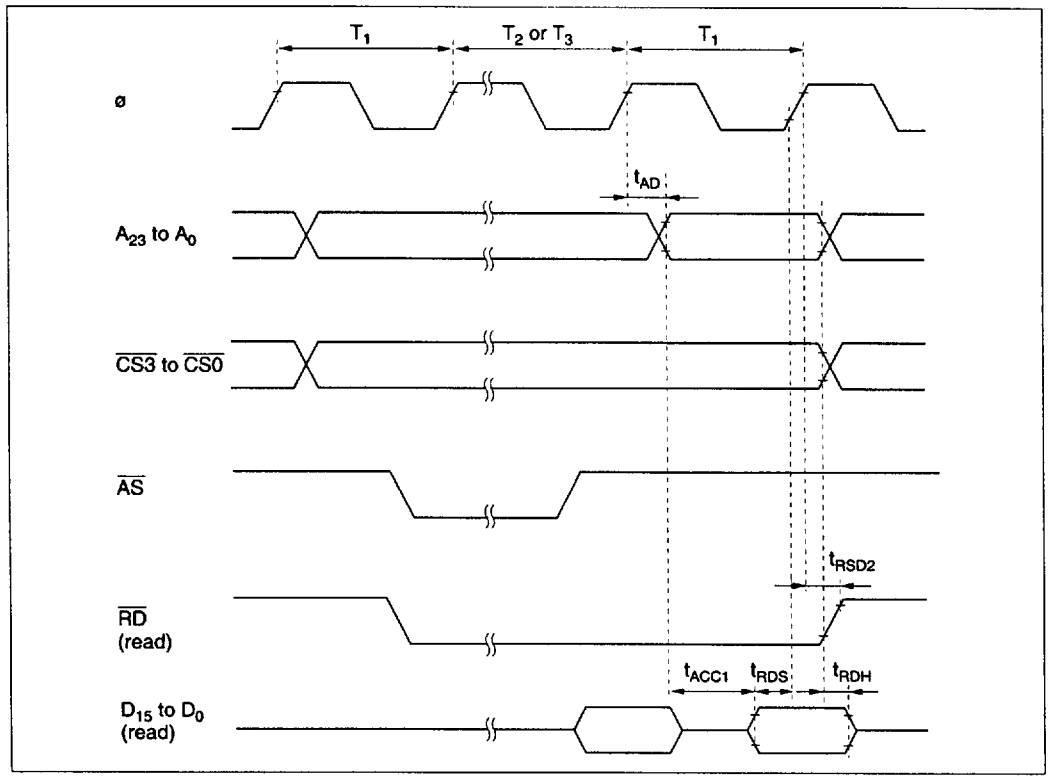


Figure 19-12 Burst ROM Access Timing (One-State Access)

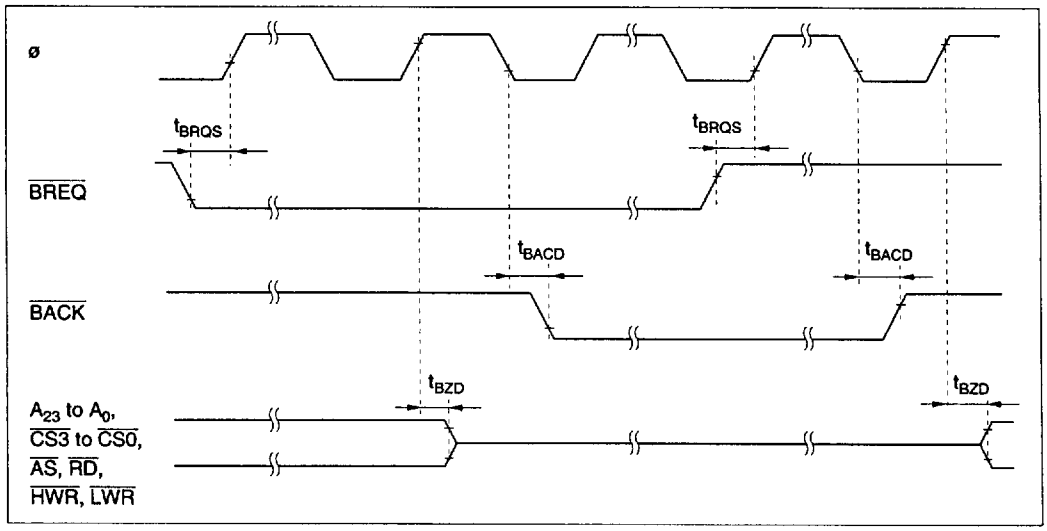


Figure 19-13 External Bus Release Timing

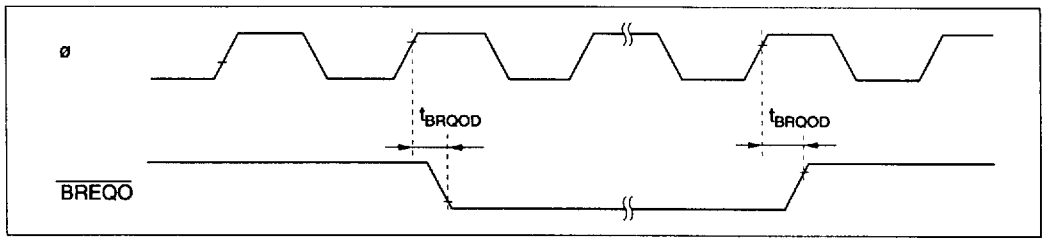


Figure 19-14 External Bus Request Output Timing

19.4.4 Timing of On-Chip Supporting Modules

Table 19-8 lists the timing of on-chip supporting modules.

Table 19-8 Timing of On-Chip Supporting Modules

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32 kHz to 10 MHz (I/O port, TMR, WDT), ϕ = 2 to 10 MHz (TPU, SCI, A/D converter), T_a = −20 to +75°C (regular specifications), T_a = −40 to +85°C (wide-range specifications)
Condition B: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 to 20 MHz, T_a = −20 to +75°C (regular specifications), T_a = −40 to +85°C (wide-range specifications)

				Condition A		Condition B			
Item			**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
I/O port	Output data delay time		t_{PWD}	—	100	—	50	ns	Figure 19-15
	Input data setup time		t_{PRS}	50	—	30	—		
	Input data hold time		t_{PRH}	50	—	30	—		
TPU	Timer output delay time		t_{TOCD}	—	100	—	50	ns	Figure 19-16
	Timer input setup time		t_{TICS}	50	—	30	—		
	Timer clock input setup time		t_{TCKS}	50	—	30	—	ns	Figure 19-17
	Timer clock pulse width	Single edge	t_{TCKWH}	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{TCKWL}	2.5	—	2.5	—		
8-bit timer	Timer output delay time		t_{TMOD}	—	100	—	50	ns	Figure 19-18
	Timer reset input setup time		t_{TMRS}	50	—	30	—	ns	Figure 19-20
	Timer clock input setup time		t_{TMCS}	50	—	30	—	ns	Figure 19-19
	Timer clock pulse width	Single edge	t_{TMCWH}	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{TMCWL}	2.5	—	2.5	—		

Table 19-8 Timing of On-Chip Supporting Modules (cont)

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32 kHz to 10 MHz (I/O port, TMR, WDT), ϕ = 2 to 10 MHz (TPU, SCI, A/D converter), T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)
Condition B: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 to 20 MHz, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

				Condition A		Condition B			
Item			**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
WDT	Overflow output delay time		t_{WOVD}	—	100	—	50	ns	Figure 19-21
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 19-22
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time		t_{TXD}	—	100	—	50	ns	Figure 19-23
	Receive data setup time (synchronous)		t_{RXS}	100	—	50	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	100	—	50	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	50	—	30	—	t_{ns}	Figure 19-24

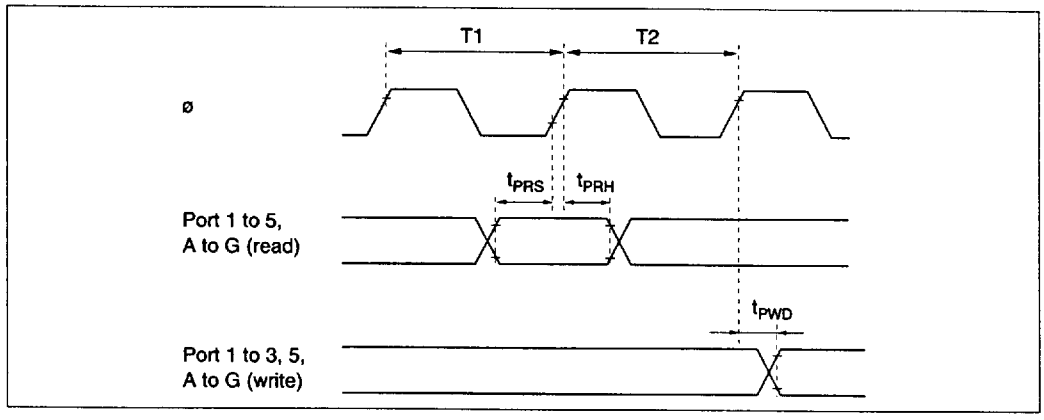


Figure 19-15 I/O Port Input/Output Timing

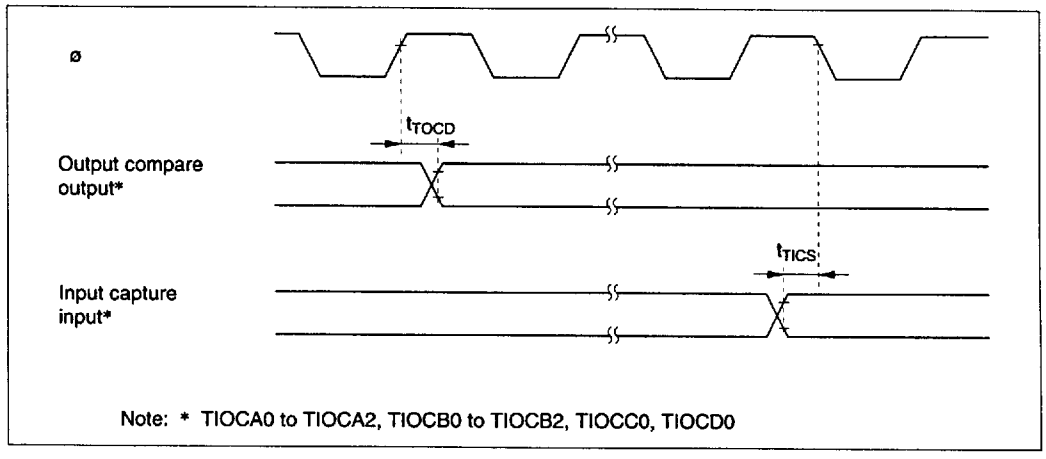


Figure 19-16 TPU Input/Output Timing

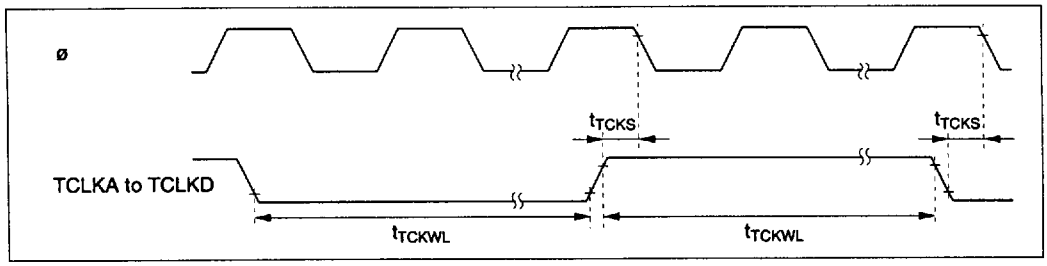


Figure 19-17 TPU Clock Input Timing

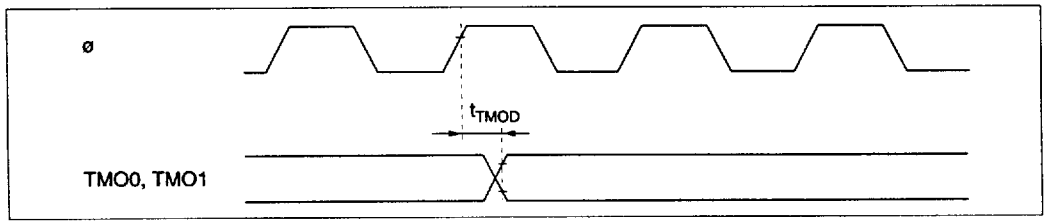


Figure 19-18 8-Bit Timer Output Timing

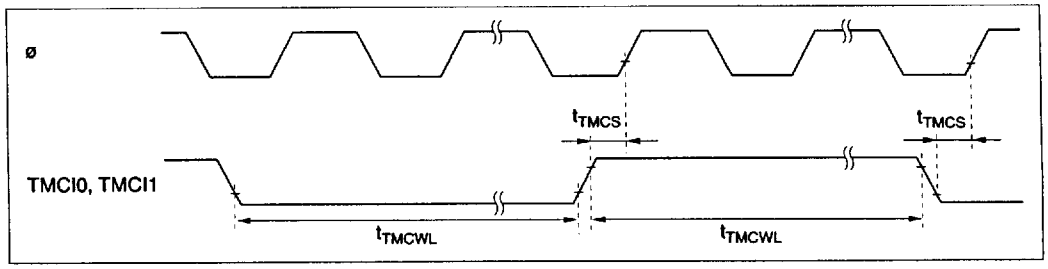


Figure 19-19 8-Bit Timer Clock Input Timing

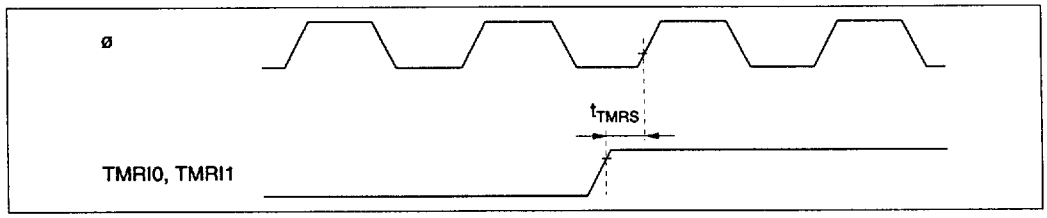


Figure 19-20 8-Bit Timer Reset Input Timing

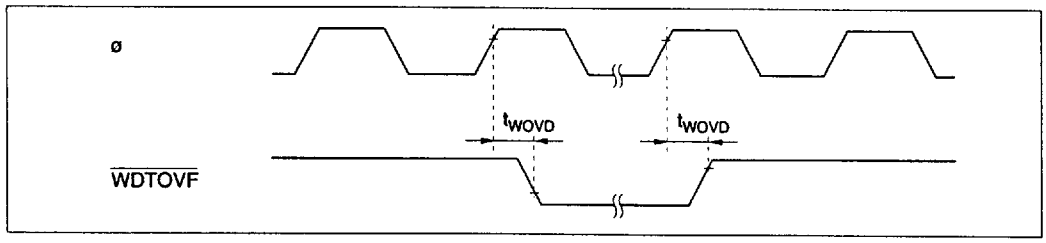


Figure 19-21 WDT Output Timing

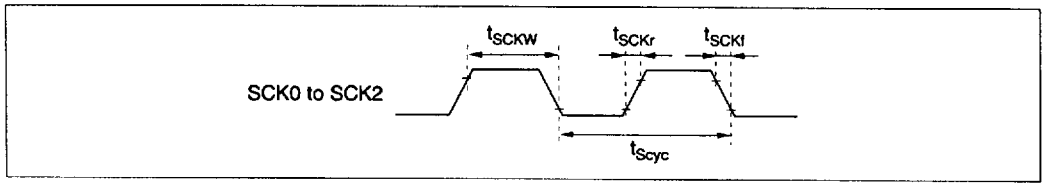


Figure 19-22 SCK Clock Input Timing

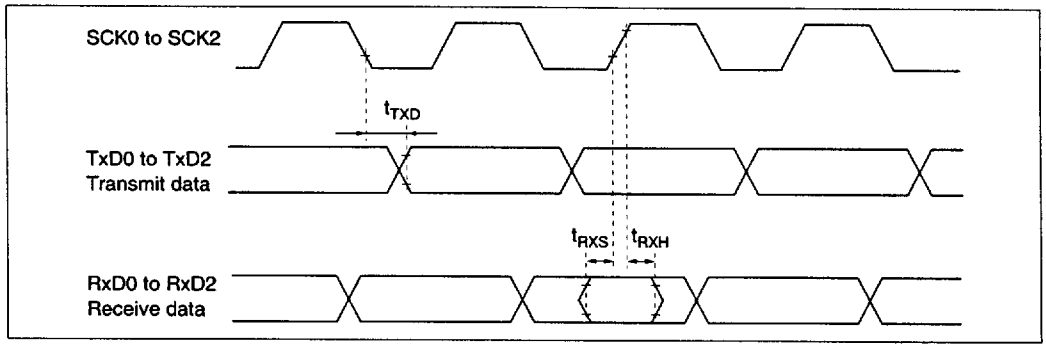


Figure 19-23 SCI Input/Output Timing Synchronous Mode

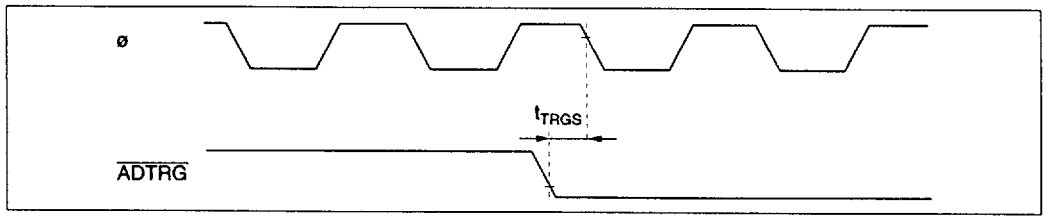


Figure 19-24 A/D Converter External Trigger Input Timing

19.5 A/D Conversion Characteristics

Table 19-9 lists the A/D conversion characteristics.

Table 19.9 A/D Conversion Characteristics

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 to 10 MHz, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 to 20 MHz, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

	Condition A			Condition B			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	bits
Conversion time	—	—	13.4	—	—	10	µs
Analog input capacitance	—	—	20	—	—	6.7	F
Permissible signal-source impedance	—	—	10*[1]	—	—	20	kΩ
	—	—	5*[2]	—	—	10*[3]	
Nonlinearity error	—	—	±6.0	—	—	5*[4]	LSB
Offset error	—	—	±4.0	—	—	±3.0	LSB
Full-scale error	—	—	±4.0	—	—	±2.0	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±8.0	—	—	±4.0	LSB

Notes: 1. $4.0 \le AV_{CC} \le 5.5$ V
2. $2.7 \text{ V} \le AV_{CC} < 4.0$ V
3. $\phi \le 12$ MHz
4. $\phi > 12$ MHz

19.6 Usage Notes

Although both the ZTAT and mask ROM versions fully meet the electrical specifications listed in this manual, due to differences in the fabrication process, the on-chip ROM, and the layout patterns, there will be differences in the actual values of the electrical characteristics, the operating margins, the noise margins, and other aspects.

Therefore, if a system is evaluated using the ZTAT version, a similar evaluation should also be performed using the mask ROM version.